CE1901 LABORATORY PROJECT

SUMMARY

In the 1960s, the integrated circuit started a new era in digital design because multiple transistor switches were now integrated together in an enclosed package called a "chip." This integration allowed computers to shrink in size and helped spark the race to outer space, the desktop calculator and eventually the personal computer revolution. Integrated transistor density has followed Moore's law throughout history. Moore's law states that the number of transistors fabricated on chip will double every two years. Table 1 shows the effect of this remarkable doubling law.

Table 1: The Growth of Integration Density

DEVICE CATEGORY	NUMBER OF TRANSISTORS	NUMBER OF LOGIC GATES	DECADE
Small Scale Integration (SSI)	10s	Just a few	mid-1960s
Medium Scale Integration (MSI)	100s	10 – 100	late-1960s
Large Scale Integration (LSI)	1000s	1,000 – 10,000	1970s
Very Large Scale Integration (VLSI)	100,000s	10,000 – 100,000	early-1980s
Ultra Large Scale Integration (ULSI)	1,000,000s+	100,000+	mid-1980s

As the number of devices fabricated on chip continues to grow according to Moore's Law, distinctions by acronym have become uncommon. Today, we routinely fabricate chips with billions of transistors but most people simply state that we are in the VLSI technology era.

While modern digital logic design practice relies extensively on computer-aided design tools and VLSI field-programmable gate arrays (FPGAs) that contain tens-of-thousands of configurable logic components, simpler digital logic chips still play a modest role in digital design. These SSI and MSI chips are used in some system level designs as "glue logic" that helps interface input devices, output devices, and memory systems to the microprocessors that form the heart of modern computing. And, because engineers optimize speed, size, power, and cost, some designs don't warrant the expense of FPGAs, microprocessors, or custom chips.

Thus, it is important that all electrical and computer engineering students know gate-level logic chips from the two historical standards. Texas Instruments created a standard family of chips called the 7400 family. RCA created a standard family of chips called the 4000 family. Each of these families contains a wide range of gates, arithmetic circuits, and other logic functions. Table 2 lists example chips from the 7400 and 4000 families. Every integrated circuit chip is identified in the industry by a unique part number. Engineering students slowly memorize the

part numbers as they complete product designs in their undergraduate classes. Note that the number of gates on the chip is given as part of the function name. Thus, a hex inverter chip has six inverters while a quad 2-input NOR chip has four 2-input NOR gates.

Table 2: Example Logic Gates from the Standard Logic Families

FUNCTION	ACRONYM	7400 SERIES CHIP	4000 SERIES CHIP
Quad 2-input NAND gates	NAND2	7400	4011
Quad 2-input NOR gates	NOR2	7402	4001
Hex Inverter	NOT	7404	4049
Quad 2-input AND gates	AND2	7408	4081
Quad 2-input OR gates	OR2	7432	4071

Over the next few weeks, students will use their FPGA boards during preliminary laboratory exercises and then use SSI/MSI chips from the standard logic families during in-lab build-wire-test exercises. This will allow you to continue refining your modern FPGA skills while also becoming familiar with the standard pin-outs of the 7400 family of chips. You will also learn to use a waveform pattern generator to apply test voltages to your circuits. And, you will learn to use a logic analyzer to verify that applied test voltages produce correct output voltages.

PRELABORATORY WORK

1. **Install** the software that will allow you to generate test waveforms from your laptop.
2. **Browse** to http://www.digilentinc.com
    a. **Click** the “Software” link in the products panel on the left hand side of the webpage.
    b. **Click** the “Download!” button next to the Waveforms software.
    c. **Run** the installer when it finishes downloading.
    d. **Use** the default install options.
    e. **Note** that the installer may determine that you need Microsoft Visual C++ runtimes installed. If it does, answer “Yes” and let it do that additional software install. It is an automatic process.
    f. **Finish** the installation.
    g. **Close** the software installer.
    h. **Close** the Waveforms software if it starts. You will not use it during your prelab work.
3. **Practice** your FPGA design, simulation, and test skills.
    a. **Make** a new Quartus schematic project.

   b. **Draw** the circuit for F(ABCD) = $\bar{A}\,\bar{B} + \bar{A}\,\bar{C} + \bar{A}\,\bar{D}$
   c. **Simulate** your design.
   d. **Analyze** the simulation diagram. **Determine** what function F(ABCD) implements. For example, does this function identify numbers between 11 and 14? Or, does it identify numbers greater than 7?
   e. **Assign** ABCD to the DE0-Nano-SOC slide switches and F to a DE0-Nano-SOC LED. **Refer** to the user manual for pin connections. The user manual is hyperlinked on the course website.
   f. **Program** the DE0-Nano-SOC board.
   g. **Use** the slide switches to test for correct operation.
4. **Prepare** a pre-laboratory exercise submission packet.
   a. **Print** your Quartus schematic and simulation waveforms. **Consult** the "printing tutorial" on the design software page of your course website.
   b. **Staple** your printouts together for easy submission. **Or consider** using Microsoft Word to create a two-page document (schematic on one page, simulation waveforms on the second page) and **print in duplex mode**. **Ask** an upperclassman or the IT helpdesk in the CC building for help printing duplex if you are unsure how to do this on the MSOE campus.
5. **Complete** the preliminary laboratory reading section of this document.

PRELIMINARY LABORATORY READING : WAVEFORMS SOFTWARE

This reading will describe the Waveforms software you installed during the prelaboratory exercises. This software is used in the EECS laboratories with a product from Digilent, Inc. called the Analog Discovery kit.

- The EECS laboratories are equipment with sophisticated laboratory instruments that are used to test electrical circuits. These instruments are designed for high-speed behavioral sampling. The EECS laboratory equipment hangs from the benches. These benches can be raised and lowered to bring the equipment up into your workspace or lower it out of your workspace. You will learn to use all of this equipment during your time at MSOE.
- The Analog Discovery kit provides a compact set of test instruments that operate at slower sampling speed. This is acceptable for most of the circuits students build in the foundational digital logic and circuit theory courses.
- The Analog Discovery kit plugs into a USB port on your computer.
- The Analog Discovery kit provides a voltage pattern generator as one instrument. A voltage pattern generator produces patterns of 0 and 1 on circuit inputs.

- The Analog Discovery kit provides a digital logic analyzer as another instrument. A logic analyzer monitors the electrical voltage on signals and draws them on a plot of voltage versus time – a timing diagram.
- The Analog Discovery kit provides a power supply. A power supply provides battery voltages to circuits under test.

PRELIMINARY LABORATORY READING : INTEGRATED CIRCUIT CHIPS

Integrated circuit chips encase a microscopic electric circuit in a plastic or ceramic case. During fabrication, industrial robots wire the internal electrical input and output signals from the microscopic circuit to metal pins on the surface of the chip. The metal pins can be organized along any number of chip sides. The arrangement of pins is known as the **package style.** When the pins are organized along the two longer sides of a rectangular shaped chip, the package style is called a **dual in-line pin** package (DIP). Figure 1 show an integrated circuit DIP chip correctly inserted into a type of prototyping environment known as a plug board or a breadboard.

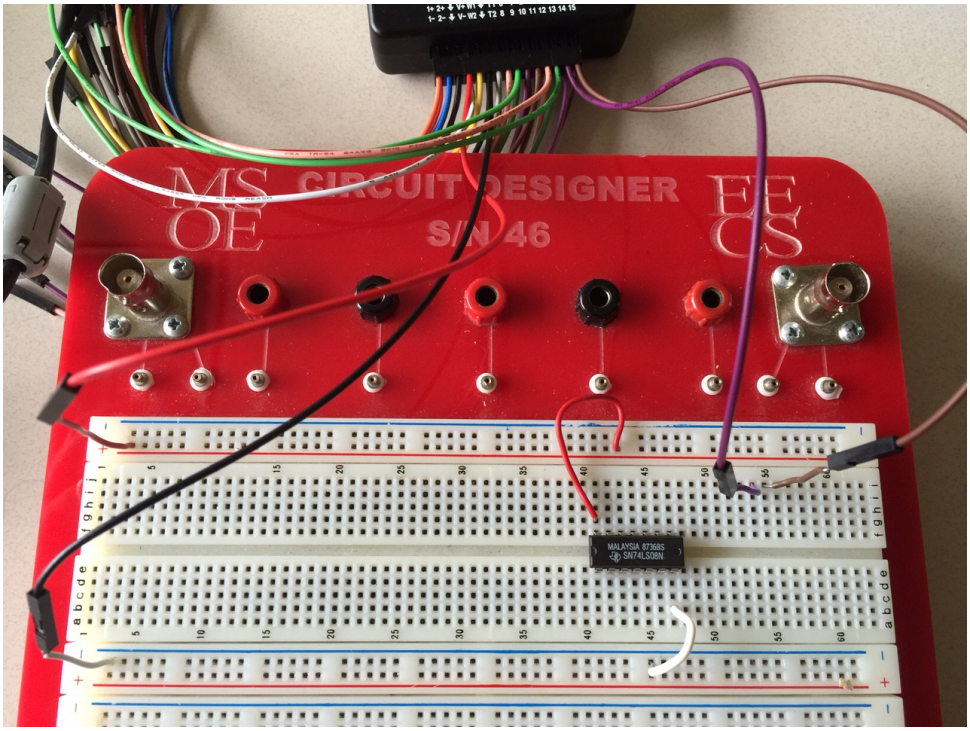

Figure 1: A Breadboard with IC

The breadboard allows electrical connections to be made without the need to heat a metal to a melting point capable of bonding items together. Instead, wires can be inserted into the breadboard holes and spring-like contacts make the electrical connections.

The plug board is divided into two halves – a top half and a bottom half. The bottom half has rows labeled **abcde** and the top half has rows labeled **fghij**. The halves are isolated from each other by a depression in the plastic – the chip gap. Each half contains sixty-four (64) columns. Each column is a unique connection node for wires and chip pins. ***Any wire or chip pin plugged into the same column is electrically connected to everything else plugged into that column.*** Each column consists of five plug points. Each plug point in a column supports only one pin or wire. Figure 2 shows these lettered rows and numbered columns.

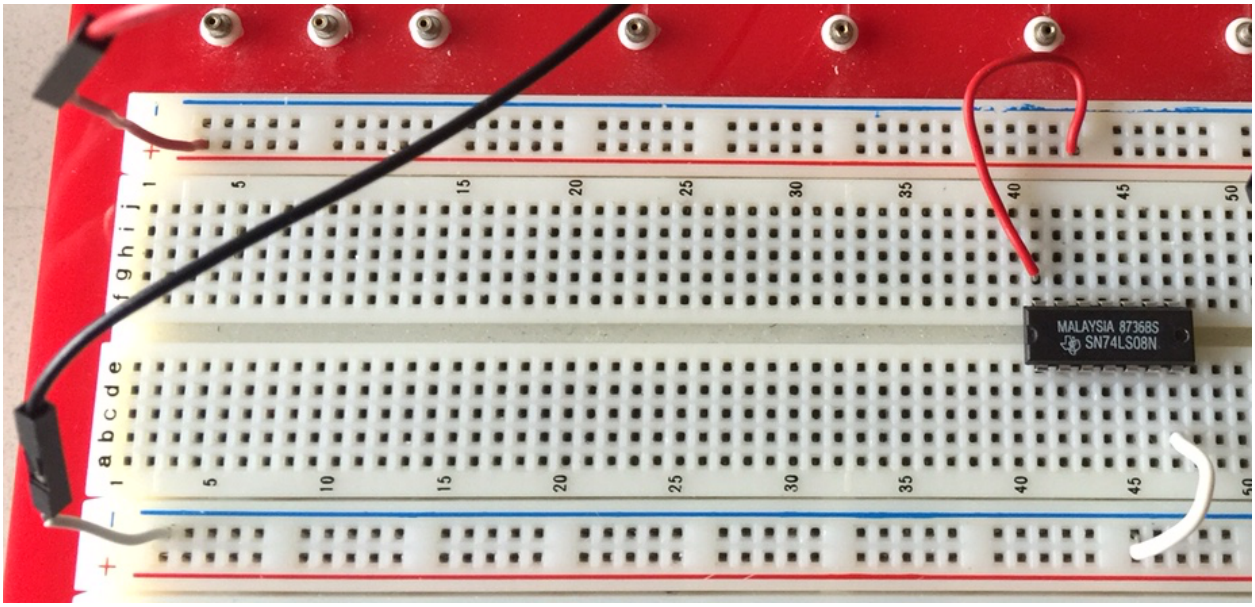

Figure 2: A Closer View of a Breadboard

Breadboards often contain power lines. In Figure 2, four power lines are visible: two red colored power lines and two blue colored power lines. Any column plug point along the power line is connected to the power line. Thus, Figure 2 shows battery power coming onto the board from the Analog Discovery Kit along the left hand side. **Red wire** is used in digital circuits to represent the hot terminal of the battery. This high energy terminal is usually called V+, VDD, VCC, or BAT+ on schematic diagrams. **Black, blue, or white wire** is used in digital circuits to represent the ground terminal of the battery. This ground terminal is usually called GND or VSS in schematic diagrams.

Thus, Figure 2 shows V+ and GND energizing “hot” and “cold” power lines running the horizontal length of the board. The IC chip sits across the chip gap with its pins aligned and inserted into unique columns. Battery power and ground have been connected to appropriate pins of the chip. Why were those pins chosen? The standard logic families place power and ground pins at standard locations on the chip. For DIP chips, power is always the pin at the upper right and ground is always the pin at the lower right. That means there must be a way of “orienting” the chip so that “top”, “bottom”, “left”, and “right” can be identified. All DIP chips have a notch cut into one short end or a depressed dot at one short end. Some chips have both a notch and a dot. The **notch always takes precedence** in chip packaging. Figure 3 shows the top of the chip up close.

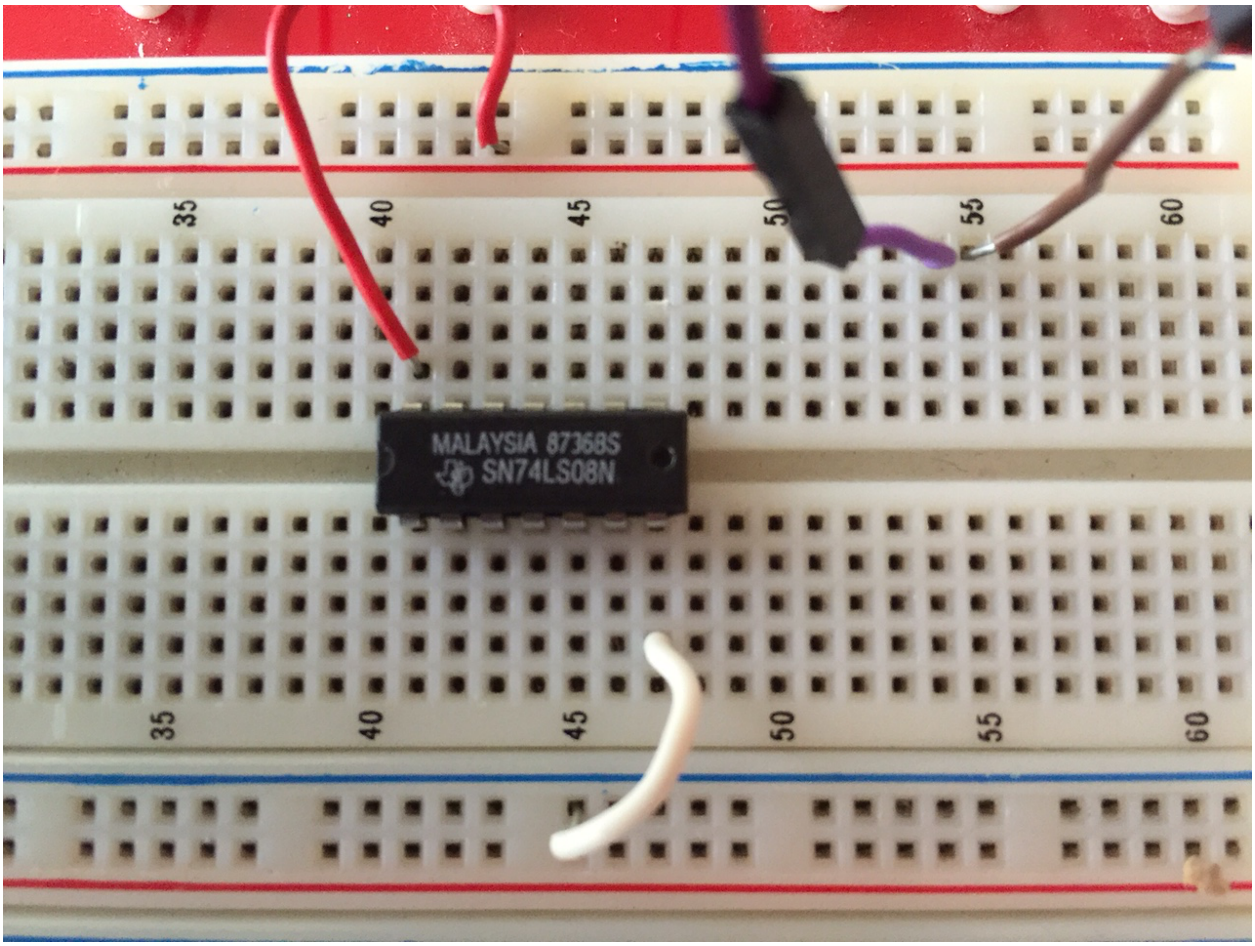

Figure 3: An Up Close View of an IC Chip

The chip in Figure 3 has both a notch and a dot. The notch takes precedence. **The notch marks the “top” of the chip**. The pins number counter-clockwise beginning to the left of the notch.

Thus, pin 1 is the top pin on the left side, pin 7 is the bottom pin on the left side, pin 8 is the bottom pin on the right side, and pin 14 is the top pin on the right side.

The top of the chip is silkscreened with its country of origin, fabrication date code, part number, and manufacturer. The date code is a 4-digit number in the format YYWW where YY represents year and WW represents the week of the year. The silkscreen of the chip in Figure 3 shows that it was fabricated in Malaysia in 1987 by Texas Instrument and is a 7408 quad 2-input AND chip. While it might seem that a 1987 chip is very old, 7400 family chips can actually last 50 to 60 years!

Chips are inserted in the breadboard by carefully bending and aligning the pins and then gently pushing downward until the chip pops into the board. Chips are removed from the breadboard by using a chip remover – a special tool that can be purchased – or by using the index fingers and thumbs on opposite long sides of the chip to gently rock it back and forth across the chip gap.

Manufacturers produce datasheets to help engineers learn important information about their chips. Datasheets usually show the gate-level logic circuit, signal-to-pin diagrams, electrical characteristics, operation temperature range, and the transistor-level circuit.

- **Review** the 7404 datasheet located on the course webpage.
- **Review** the 7408 datasheet located on the course webpage.
- **Review** the 7432 datasheet located on the course webpage.
- **Review** these key points about wiring chips.

KEY POINTS

Wiring is a skill that comes with practice. Remember these key points:

- each column is the ***same*** connection node
- a plug point supports only one wire or pin
- use intermediate columns to jump multiple wires to finish a connection
- use shorter wires and keep the wiring tight against the board

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PRELIMINARY LABORATORY READING : USING THE WAVEFORMS SOFTWARE

This reading will describe using the Waveforms software. The Waveforms software **cannot be started without an instrumentation kit**. Thus, read this material before lab to become familiar with the software. But, you will not be able to follow along by using the software at home. Instead, **use** this reading material as reference during the laboratory period.

1. **Start** Waveform. The software will present you with an instrument panel if an instrumentation kit is connected. The instrumentation panel is shown in Figure 4. Each instrument has a push button that opens its control panel.

Figure 4: The Waveforms Instrument Panel

2. **Push** the buttons for voltage (power supply), patterns, and analyzer. **Organize** your instrument control panels so that they appear on screen as shown in Figure 5. The instruments in Figure 5 clockwise from upper left are: logic analyzer, power supply, instrument panel, and pattern generator.

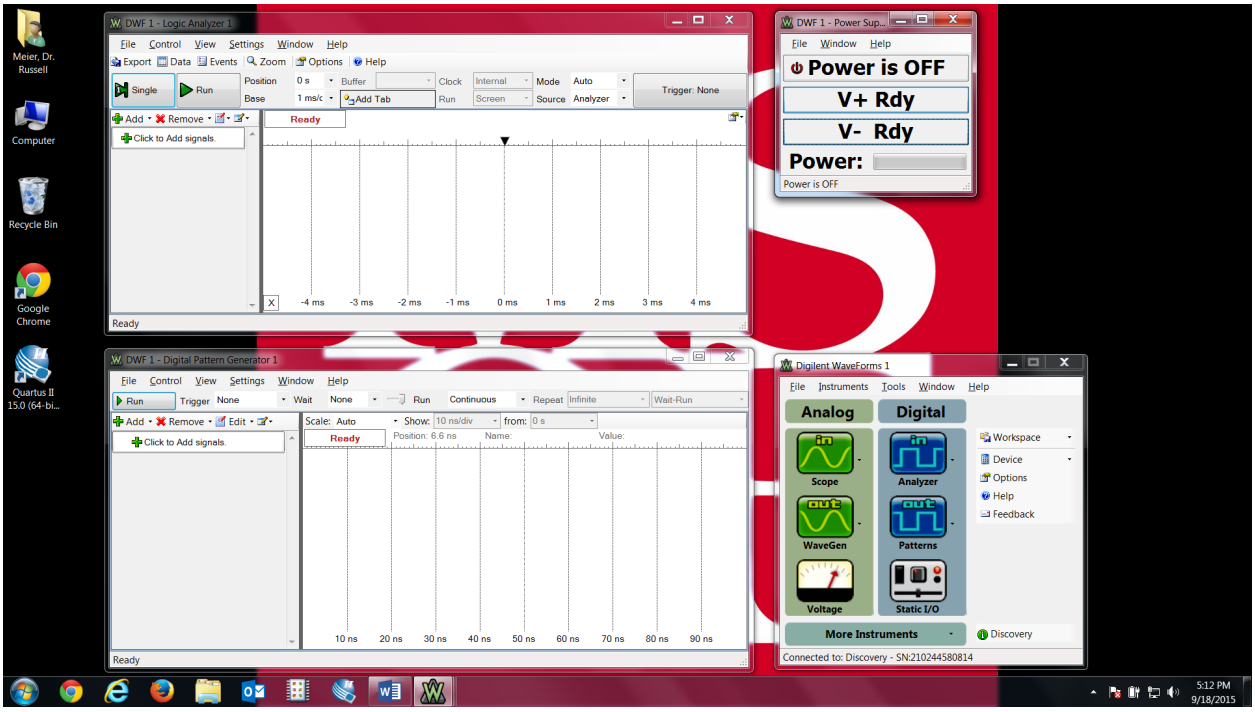

Figure 5: Waveforms with Visible Logic Analyzer, Voltage, and Pattern Generator Instruments

3. **Remember** that all integrated circuit chips need battery power. They cannot gate energy on or off signal wires unless energy is provided! The **voltage panel** allows you to turn on a +5V battery called V+. The panel also allows you to turn on a -5V battery called V-. **Digital IC chips do not use negative voltage.** Thus, the V- battery will ***never be used*** in this course. Also **remember** that good wiring practice encourages all wiring be completed before turning batteries on.
4. The **pattern generator panel** allows you to create patterns of voltages to apply to circuit inputs. Signals and signal sets (**busses**) can either have arbitrary logic values or coordinated values like binary count sequences written onto them through time.
5. The **logic analyzer panel** allows you to create signals and sets of signals to be monitored and displayed through time. In general, you apply inputs with the pattern generator and monitor outputs with the logic analyzer. The logic analyzer can simultaneously display inputs and outputs on one comprehensive voltage-versus-time graph – called a timing diagram.

6. **Build** the circuit shown in Figure 6.
    a. The chip is the 7408 quad 2-input AND.
    b. Power (V+) is brought from the instrumentation kit to the breadboard. It is attached to the red power line. The 7408 chip is wired to power.
    c. Ground is brought from the instrumentation kit to the breadboard. It is attached to the blue power line. It is marked on the instrumentation kit with something similar to this standard ground symbol (▼) but it looks more like a downward pointing arrow because it also shows a bit of wire connected to it. The instrumentation kit provides four connections to ground – each of them a black wire. The 7408 chip is wired to ground.
    d. Digital input/output (DIO) signals 6 and 7 are brought to the board as AND gate inputs A and B. These are the purple and brown wires seen in the right hand side of the figure. These signals are wired to 7408 pins 1 and 2 because the datasheet shows pins 1 and 2 as the two inputs of the AND gate.
    e. Digital input/output signal DIO1 is wired to the AND gate output on pin 3.

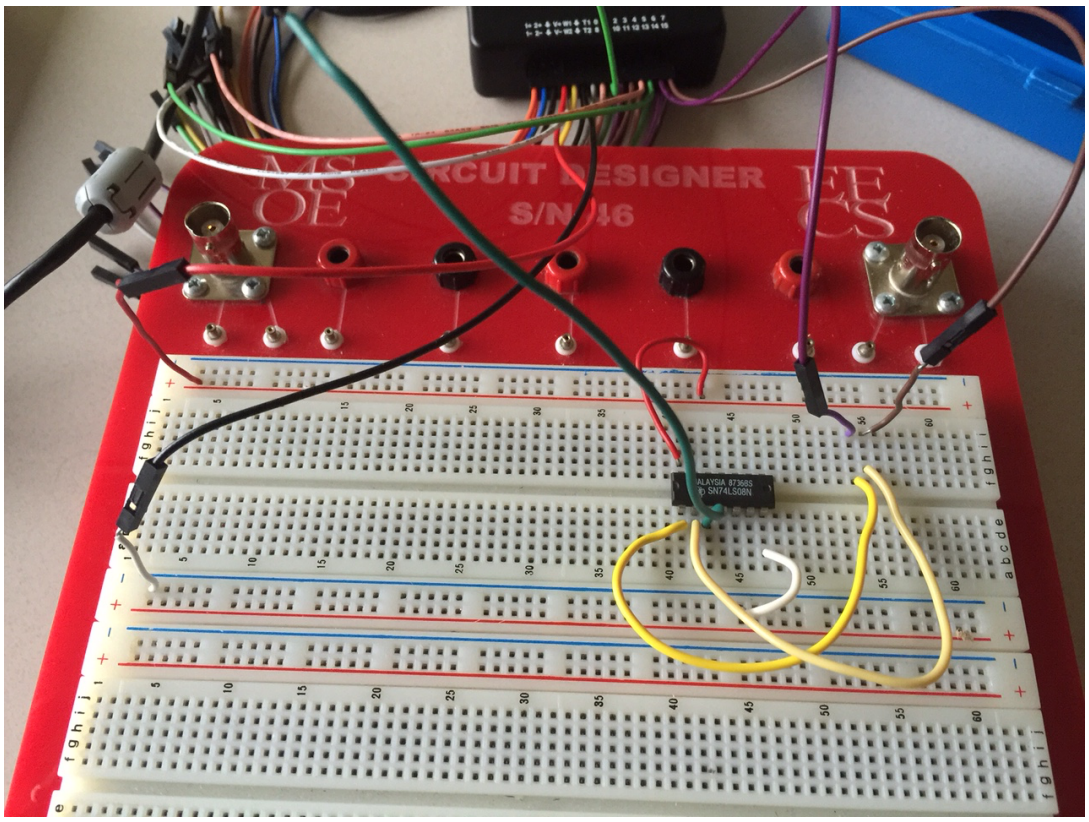

Figure 6: A 7408 AND IC Ready for Testing

7. **Configure** the pattern generator to generate voltages for circuit inputs A and B.
    a. **Add** a signal bus. **Do not** add an "empty bus."
    b. **Add** digital input/output signal DIO6 to the "selected" column.
    c. **Add** digital input/output signal DIO7 to the "selected" column.
    d. **Note** that the most significant bit was the first added to the "selected" column.
    e. **Push** the "constant" label in the "type" column. A pop-up menu appears.
    f. **Select** "binary counter."
    g. **Click** "ok" to finish adding the bus. A 2-bit number line appears on signals DIO6 and DIO7. Remember that these signals are wired to AND gate input A and AND gate input B.
8. **Configure** the logic analyzer to monitor the circuit inputs and outputs.
    a. **Add** a signal bus. **Do not** add an "empty bus."
    b. **Add** DIO6 to the "selected" column.
    c. **Add** DIO7 to the "selected" column.
    d. **Click** "ok" to finish adding the bus.
    e. **Add** a signal.
    f. **Add** DIO1 to the "selected" column.
    g. **Click** "ok" to finish adding the signal.
9. **Compare** your work to Figure 7.

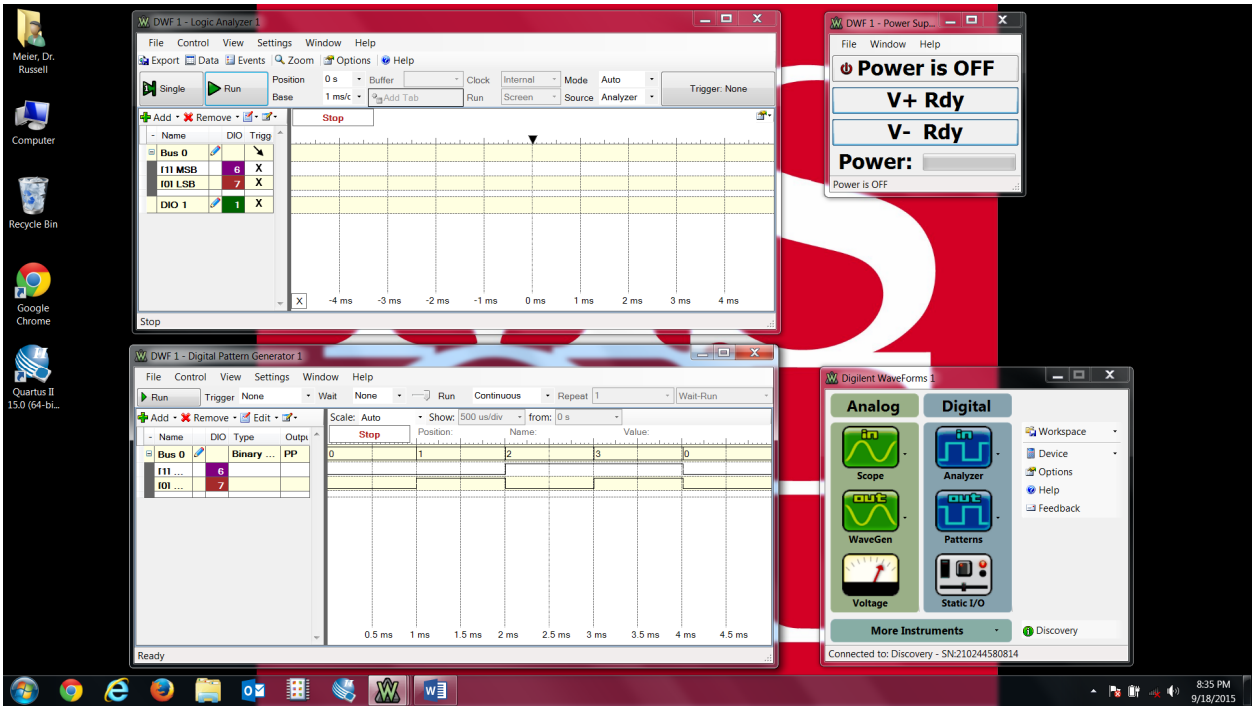

Figure 7: Instruments Ready to Test the 7408 AND Gate

10. **Run** the circuit test.
    a. **Click** the on/off button on the power supply to turn on the batteries. **Note** that there may be a "current surge" error message when the power supply is first turned on. If this occurs, try again. Multiple tries hint at circuit wiring errors.
    b. **Click** the "run" button on the pattern generator to begin applying voltages to the circuit.
    c. **Click** the "run" button on the logic analyzer to start sampling the circuit inputs and outputs in order to create a timing diagram.
    d. **Wait** a couple of seconds.
    e. **Click** the "stop" button on the logic analyzer to stop sampling and present a final timing diagram.
    f. **Verify** that the AND gate is functioning by comparing your logic analyzer timing diagram against the AND truth table. The timing diagram should look similar to Figure 8.

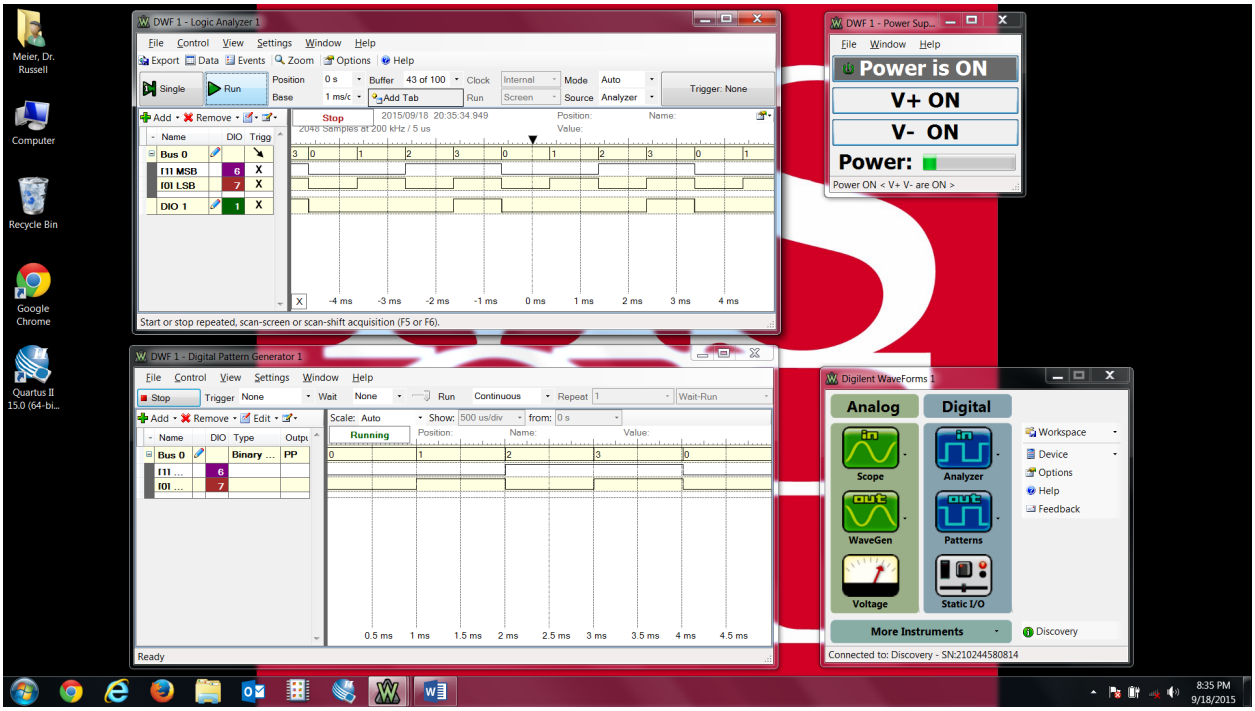

Figure 8: The Completed 7408 AND Gate Test

    g. **Note** that this simple circuit test could become much more complex. There are numerous options that can be set to control the test. You will learn more about these "trigger conditions" in later laboratories and courses.

h. **Note** that the other three gates in the 7408 chip could be similarly tested to ensure they were operational. While you do not have to do this for this laboratory exercise, the process is simple. The DIO6 and DIO7 input wires would move to the next 7408 gate's input pins and the DIO1 output wire would move to the output pin. Continue through all gates. **Use** the 7408 data sheet to identify input-output pin sets by gate.

11. **Take a screenshot** to document your work.
    a. **Use** keyboard combination Function-PrtSc.
    b. **Paste** the image into Microsoft Word as a figure with an appropriate label such as "Test of 7408 AND Gate."
12. **Stop all instruments** and **tear down** the circuit.
    a. **Click** to "stop" the logic analyzer and pattern generator.
    b. **Turn off** the power supply.
    c. **Remove** circuit wires and gently rock the chip using your thumb and fore-finger on the long-sides of the chip. **See** Figure 9 for an example of removing a chip.

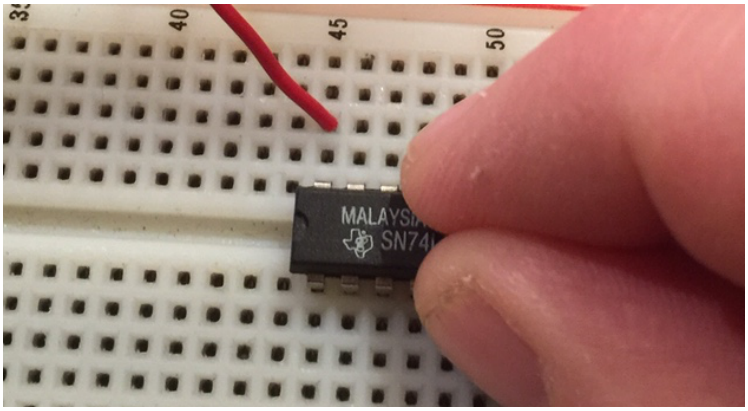

Figure 9: Removing an IC Chip by Rocking Gently on the Long Sides

This completes the preliminary reading.

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DELIVERABLES DUE DURING THE LABORATORY PERIOD

Complete these exercises during the laboratory period.

1. **Demonstrate** your prelaboratory DE0-Nano-SOC circuit.
2. **Choose** a laboratory partner to work with.
3. **Go** to EECS Tech Support and **check out** one set of equipment per team.

Table 3: Required EECS Tech Support Equipment

ITEM	QUANTITY
74LS04	1
74LS08	1
74LS32	1
Blue Wire Kit	1
Analog Discovery Kit	1
Circuit Design Breadboard	1

4. **Complete** the Waveforms tutorial from the preliminary laboratory reading. **Work together** to build, wire, and test the 7408 circuit. **Demonstrate** to the instructor.
5. **Build-wire-test** a mystery circuit and use Waveforms to analyze its behavior.
    a. **Use** the schematic diagram shown in the reference figures at the end of this lab packet to guide your work. The mystery circuit is Figure 11.
    b. **Note** that the schematic shows chip numbers and suggested pin numbers. **Refer** to the 7400 family datasheets to see how the pin numbers were chosen. Each chip has multiple gates. Chip gates are simply assigned to schematic gates one at a time. Each gate's pins are added to the diagram. The diagram then guides wiring. Figure 10 shows powers, grounds, and wires interconnecting pins.

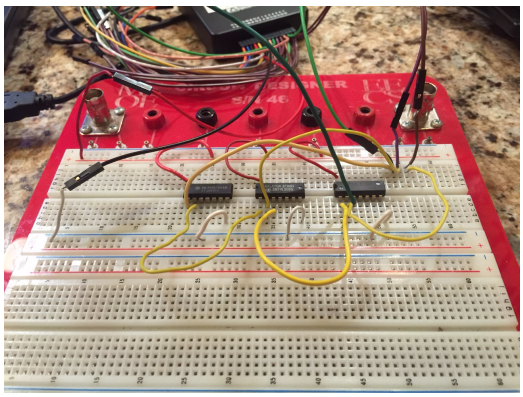

Figure 10: Multiple Chips Interconnected with Wire

c. **Test** and **verify** the circuit using the Analog Discovery Kit.
    i. **Use** DIO signals DIO4, DIO5, DIO6, and DIO7 as circuit input voltages.
    ii. **Use** DIO signal DIO1 to sample the circuit output.
    iii. **Use** a count sequence to apply all 15 number line values.
    iv. **Determine** the function by examining the output. For example, is the function Y(ABCD) = 1 if ABCD > 11?
d. **Take** a screenshot to document your work.
e. **Demonstrate** your work to the instructor.

6. **Stop all instruments** and **tear down** the circuit.
    a. **Click** to "stop" the logic analyzer and pattern generator.
    b. **Turn off** the power supply.
    c. **Remove** circuit wires and gently rock the chips using your thumb and fore-finger on the long-sides.
7. **Build-wire-test** a greater-than-4 detector.
    a. **Use** the schematic diagram shown in the reference figures at the end of this lab packet to guide your work. The greater-than-4 detector is Figure 12.
    b. **Note** that the schematic has chip numbers and suggested pin numbers shown. **Refer** to the 7400 family datasheets to see how the pin numbers were chosen.
    c. **Test** and **verify** the circuit using the Analog Discovery Kit.
        i. **Use** DIO signals DIO4, DIO5, DIO6, and DIO7 to provide circuit input voltages.
        ii. **Use** DIO signal DIO1 to sample the circuit output.
        iii. **Use** a count sequence to apply all 16 number line values.
        iv. **Compare** the output energy to the energy expected for greater-than-4 identification.
    d. **Take** a screenshot to document your work.

   e. **Demonstrate** your work to the instructor.
8. **Stop all instruments** and **tear down** the circuit.
   a. **Click** to "stop" the logic analyzer and pattern generator.
   b. **Turn off** the power supply.
9. **Remove** circuit wires and gently rock the chip using your thumb and fore-finger on the long-sides of the chip.
10. **Return** your EECS Tech Support equipment.

DEMONSTRATION AND SUBMISSION

1. **Demonstrate** each functioning circuit to the instructor during the laboratory period.
2. **Generate** a PDF document for each test.
3. **Submit** your PDF documents through your instructor's preferred submission method.

REFERENCE FIGURES

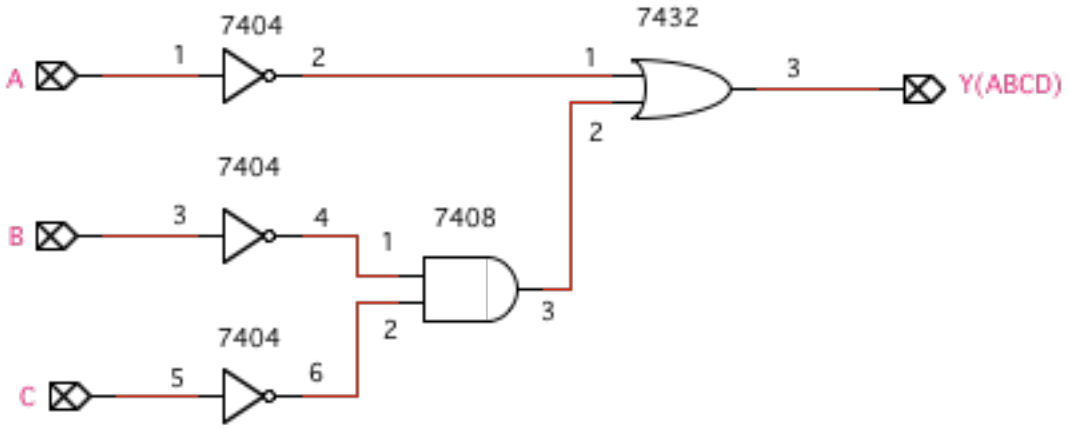

Figure 11: Mystery Circuit

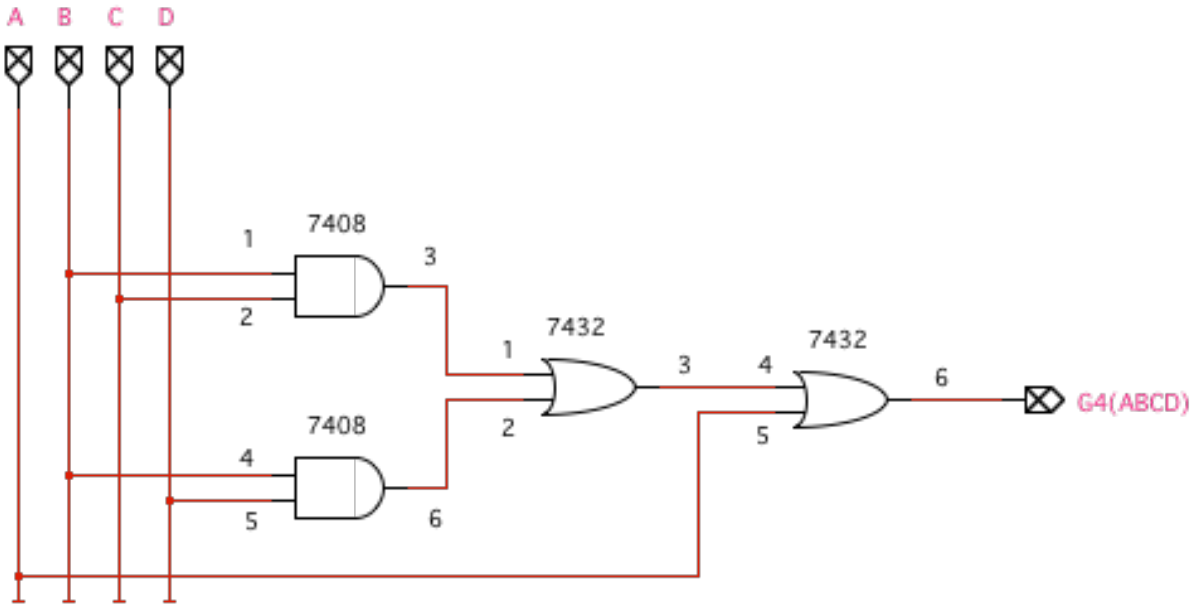

Figure 12: Greater-than-4 detector